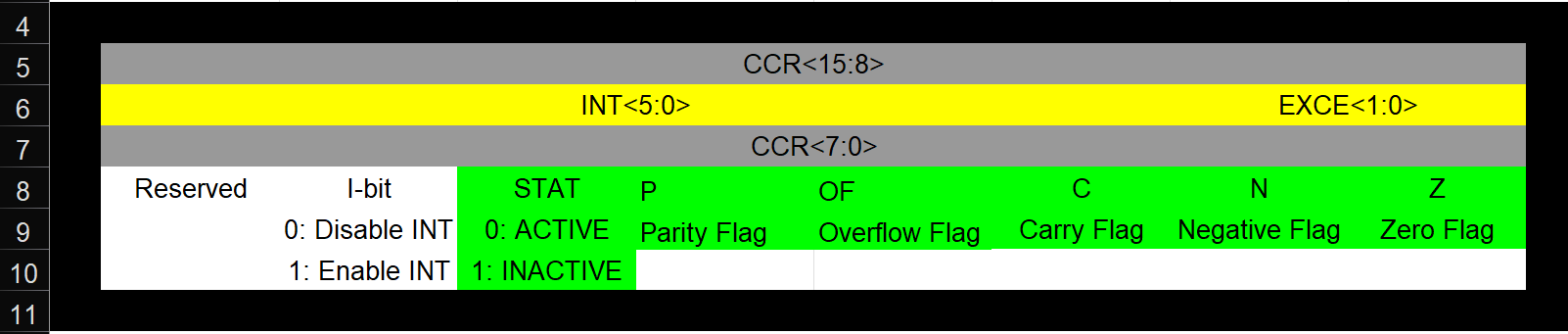
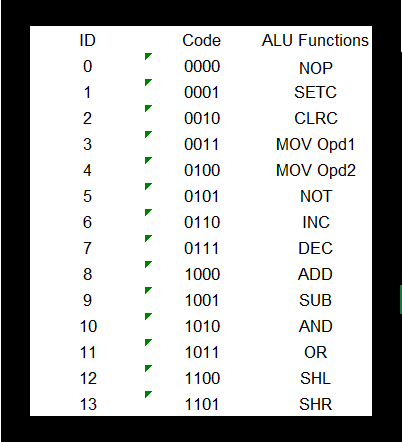
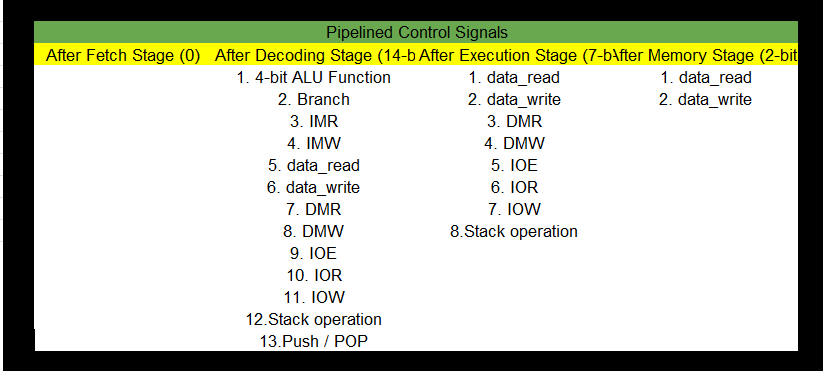
Phoenix Processor

|  |  |  |
| --- | --- | --- |
| Ahmed Alaa El-Sayed Arabi | 1 | 7 |
| Abdelrahman Hamza | 1 | 37 |
| Ahmed Sabry | 1 |  |
| Ahmed Sayed | 1 |  |

1. **Instruction Categories:**
   1. Zero Operand
   2. One Operand
   3. Two Operands
   4. Memory Operation
   5. Control Operations
   6. Input Signals



1. **CCR Flags:**
2. **ALU Functions:**
3. **Control Unit Signals:**
4. **Pipeline Hazards:**

|  |  |  |  |
| --- | --- | --- | --- |
| Hazards Types | Hazard Location | Occurrences Detection | Hazard Solution |
| Data Hazard | M-D | Old\_Rdst = New\_Rsrc (ALU Operation) | Data Forwarding |
| Data Hazard | W-D | Old\_Rdst = New\_Rsrc (ALU Operation) | Data Forwarding |
| Data Hazard | Load Use (M-D) | Old\_Rdst = New\_Rsrc (DMR is activated) | HW Stalling One Cycle + Data Forwarding |
| Data Hazard (Interrupt Context Switch) | W-D | Old\_Rdst = New\_Rsrc (ALU Operation) | Data Forwarding |
| Data Hazard (Interrupt Context Switch) | Load Use (M-D) | Old\_Rdst = New\_Rsrc (DMR is activated) | HW Stalling One Cycle + Data Forwarding |
| Control Hazard | E | Assumed Not Taken, But Taken Branch | Flush Pipelines |